LV Converters: Improving Efficiency and EMI Using Si MOSFET MMC and Experimentally Exploring Slowed Switching

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Nina M. Roscoe, Derrick Holliday, Neville McNeill, and Stephen J. Finney

***Abstract*—Widespread adoption of electric vehicles will require AC power distribution systems to accommodate high penetrations of power electronic loads, placing increasing demands on the power quality of grid-connected converters. Recent developments in devices and circuit topologies have potential to improve the intrinsic power quality of these grid interface inverters, reducing the need for passive filters and associated reactive power consumption. Wide bandgap devices, such as SiC, have recently gained much attention due to their low switching losses facilitating raised PWM frequencies. However the high cost of SiC together with electromagnetic interference (EMI) resulting from very rapid switching transitions necessary to realize low switching losses cause concern. Previous research in Si MOSFET modular multilevel converters (MMC) suggests a high efficiency alternative with potential for lower EMI. Si MOSFET MMC benefits are enhanced with parallel-connected devices and slowed switching, made possible by low effective switching frequency. This paper uses experimental results to explore the impact of parallel connection and slowed switching on Si MOSFET MMC losses, and presents improved Si MOSFET switching loss models to resolve inaccuracies observed with conventional Si MOSFET models. EMI is then compared between SiC and Si MMC using carefully controlled relative measurements of radiated EMI.**

***Index Terms*— Energy Efficiency, EMI, MMC, Si MOSFET, SiC MOSFET**

I. Introduction

ACHIEVING high efficiency with low harmonic distortion and low electromagnetic interference (EMI) is increasingly critical for grid connected converters as power electronic loads increasingly dominate [1-3]. Electric vehicle (EV) charging particularly threatens grid stability with very high expected volumes demanding low distortion, EMI compliant, highly efficient and preferably bi-directional AC/DC converters [4-6].

Improved harmonic performance can be achieved using the shaped waveforms generated by modular multilevel converters (MMC), or by implementing careful filtering on 2-level converters. SiC devices improve 2-level converter efficiency even whilst operating with increased switching frequency, thus also reducing filter bulk, loss and cost [7-10], compared with traditional IGBT 2-level converters. However, increased efficiency brought by SiC comes with the risk of increased EMI caused by the rapid switching transients, combined with the greater EMI generated as switching frequency is increased in order to reduce filter loss and bulk. Hence the increased efficiency of the SiC 2-level converter can only be achieved at the cost of EMI performance. Any attempt to slow the SiC switching will impact on switching loss. EMI shielding and filtering can ensure the SiC converter is EMC compliant, but besides the cost and volume of the extra components this activity introduces significant design costs.

MMC by contrast remove the need for a DC-side filter altogether and reduce AC-side filtering. MMC decouple harmonic performance and switching frequency. At the same time experimental measurements suggest that MMC suffer considerably lower loss than SiC 2-level converters, particularly when parallel connection is used to reduce conduction loss [11-14]. Besides achieving good harmonic performance at low switching frequency leading to lower EMI, MMC cells also switch smaller voltages potentially bringing another drop in EMI. MMC switching loss is negligible compared with conduction loss [11-13] allowing the possibility of slowed switching, and initial experiments demonstrate reduced dv/dt, di/dt and ringing [11-13] as switching slows. Reduced switching transients, when combined with smaller ringing amplitude and lower switching frequency, are all expected to reduce EMI generated by converters.

This paper discusses the influence of switching frequency, voltage switching level, dv/dt, di/dt, and ringing amplitude on the amplitude of radiated EMI. Experimental measurements of EMI are then compared for an SiC 2-level converter and an Si MOSFET MMC single cell designed for use in a 7-level

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MMC. Both converters are designed to optimize efficiency. The effect of switching frequency, switching voltage and slowed switching (for Si MOSFET MMC) are experimentally demonstrated and compared with theoretical predictions.

Both the SiC 2-level converter and the Si MOSFET MMC are suited to the bidirectional operation necessary to support low carbon electrical supply using energy storage in the form of Vehicle-to-Grid (V2G) energy transfer. Furthermore, it is noted that SiC MOSFET gate drive must be bipolar in order to achieve optimum performance [7-10,15], with careful design to prevent over- or under-voltage on the gate [15] and to reduce parasitic-induced oscillations [9]. Destruction as a result of unwanted device turn-on is of far greater risk in SiC MOSFETs compared with Si MOSFETs [15,16], while gate oxide reliability has been a challenge to SiC [17,18] with some improvement in gate oxide tolerance to temperature more recently [7].

A critical aspect of using slowed switching in the low voltage MMC to improve EMI performance is that the increased switching losses caused by the slowed switching must not erode efficiency to an unacceptable degree. The effect of parallel connection and slowed switching on loss is investigated experimentally, and compared with results obtained using loss modelling. As a result the loss model required improvement as previous modelling did not successfully predict the effect of slowed switching or parallel connection. Therefore, an improved loss model is also presented for Si MOSFET switching.

The paper is organized as follows: in Section II the Si MOSFET MMC and SiC 2-level converter topologies are outlined and defined; in Section III a Si MOSFET switching loss model is presented, which is important when analyzing the effects of slowed switching and parallel-connection on converter performance; in Section IV the impact of slowed switching on Si MOSFET MMC converter efficiency is explored as well as comparing Si MOSFET MMC and SiC 2-level converter efficiency; in Section V EMI measurements are presented, showing the effects of switching frequency, slowed switching, multiple cells with interleaved switching and comparing SiC and Si MMC EMI; in Section VI the volume and cost of SiC and Si MMC converters are compared; and finally conclusions are presented in Section VII.

II. AC/DC Converters for EV Charging

It is assumed for this research that the EV charger will be grid-connected through 3-phase, 415 V_{rms} AC/DC converters with a minimum power of 10 kW, and that all individual harmonics will be maintained below 5 % on both the AC- and DC-side. DC voltage is taken to be 750 V, meaning that 3rd harmonic injection is not required and allowing for up to 10 % voltage tolerance on the AC-side. Switching frequency is not constrained, and is therefore chosen for optimum converter performance.

The baseline performance comparison for the Si MOSFET MMC has been taken to be an SiC 2-level converter, optimized using previously reported techniques [21]. The SiC MOSFET chosen is the C2M0045170D, with 2 parallel-connected devices, and operated at 18-kHz switching frequency, which is found to deliver optimum efficiency for a 2-level SiC converter [21]. The circuit diagram for the SiC converter is shown in Fig. 1.

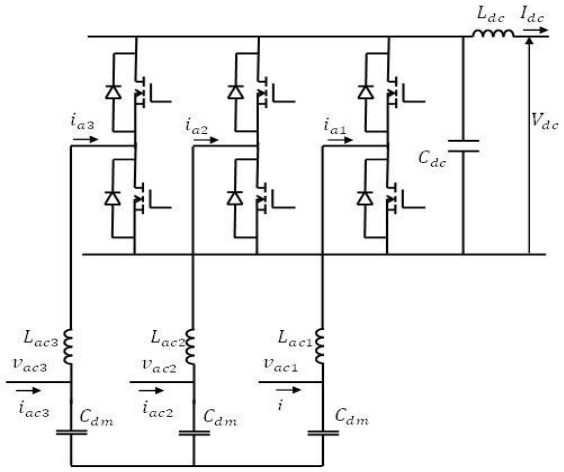


Fig. 1. 3-phase 2-level half-bridge SiC MOSFET 2-level converter, with AC- and DC-side filtering

Previous investigation of the Si MOSFET MMC [11-14] has shown that conduction losses dominate switching loss due to low effective cell switching frequency. One phase leg of a 3-phase 5-level Si MOSFET MMC converter is shown in Fig. 2.

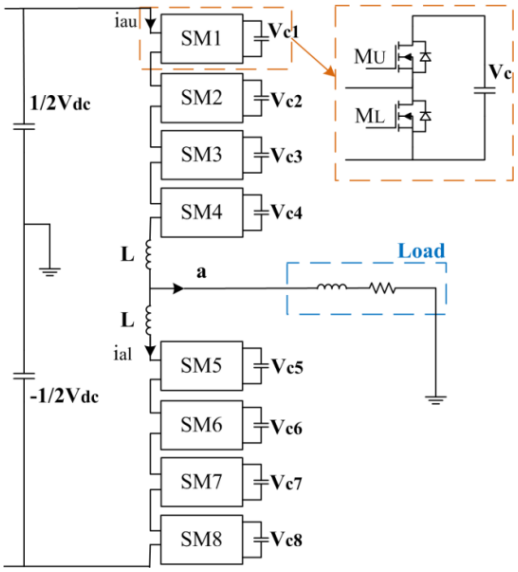


Fig. 2. A single phase leg of a 3-phase 5-level Si MOSFET MMC, using half-bridge cells for minimum conversion loss

The prevalence of conduction losses in MMC makes parallel connection of MOSFETs attractive in order to reduce on-state resistance and hence reduce conduction loss. However, previous studies [11-14] did not include measured switching losses as Si MOSFET parallel connection was increased, so measured Si MOSFET switching losses will be explored in this paper. In addition, the possibility of reducing EMI using slowed switching was proposed [11], with modelled losses suggesting that switching could be considerably slowed without impacting overall converter loss.

This paper uses experimental data to explore the impact of slowed switching on Si MMC loss.

III. Si MOSFET Switching Loss

A. Measuring Loss and Comparing with Standard Si MOSFET Switching Loss Models

As a first step, switching loss in an Si MOSFET half-bridge of suitable rating for use in LV MMC was measured. In order to measure loss effectively in the Si MOSFET half-bridge, the switching frequency was chosen as 20 kHz, to ensure that switching loss was not negligible compared with conduction loss. Heatsink thermal resistance was calibrated by applying DC voltage and current to the Si MOSFET switches, and used to correlate temperature rise with dissipated power during switching. The resulting loss is compared with the standard loss model [11-13], see Fig. 3. For a 3-phase, 7-level MMC converter delivering 10 kW at a DC voltage of 750 V, each cell must conduct a peak current of approximately 19 A, and cell voltage is 125 V. The IRFP4668 MOSFET [22] offers optimally low on-state resistance with sufficient voltage rating for safe operation at 125 V. During each measurement, temperature took up to two hours to reach equilibrium.

The standard loss model for Si MOSFET switching is given by equations (1)-(4) [11] .

$$P_{SW} = \frac{1}{2} I_{DS} V_{DS} (t_{off} + t_{on}) f_s \quad (1)$$

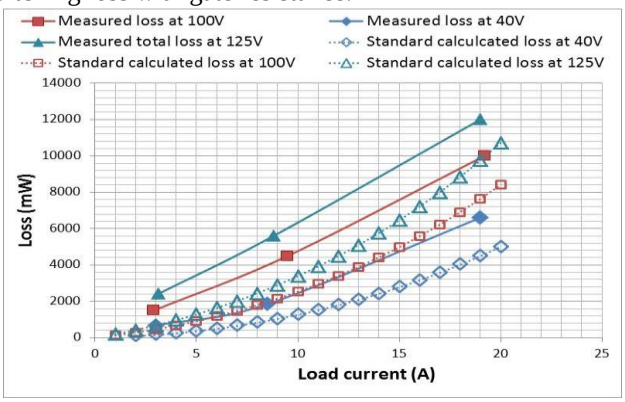
$$t_{on} = t_{off} = \frac{Q_{SW}}{I_{GS}} \quad (2)$$

$$I_{GS} = \frac{V_{gg} - V_{miller}}{R_g} \quad (3)$$

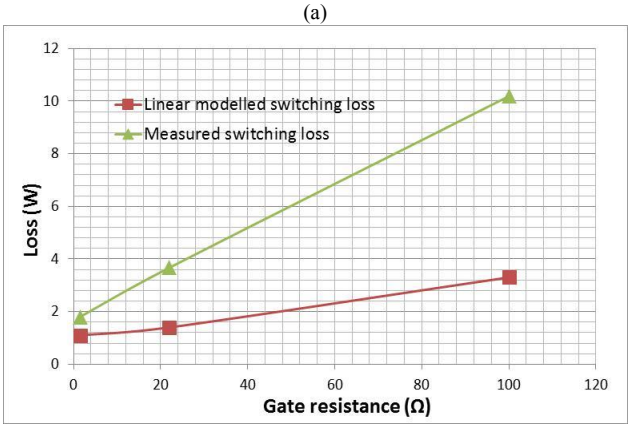
$$P_{rr\_D} = Q_{rr} V_{dc} f_s \quad (4)$$

I_{DS} is drain-source current, V_{DS} is drain-source voltage, f_s is switching frequency, t_{on} and t_{off} are turn-on and turn-off time respectively, Q_{sw} is switching gate charge and I_{GS} is average gate current during switching, V_{gg} is gate-drive voltage, V_{miller} is the Miller voltage, Q_{rr} is reverse recovery charge in the body diode and V_{dc} is the DC voltage applied to the half-bridge. In general it is assumed that Q_{rr} scales linearly with current and voltage, and an estimate must be made as to the correct rate of change of current in order to select the correct starting value for Q_{rr} from the data sheet. In this case, switching for the single device was fast enough to require that Q_{rr} be selected from the upper end of the range of reverse recovery charge.

Initially this loss model was compared with measured results for single IRFP4668 devices in a half-bridge, to confirm the effectiveness of the switching loss model. Conduction loss was measured using DC voltage and current, to ensure that predictions of on-state resistance were correct. It was discovered that the on-state resistance was approximately 2-mΩ higher than expected at room temperature, of which a small proportion may be attributed to tracking resistance, but the remainder is assumed to be component tolerance, suggesting device on-resistance is close to the maximum specified value of 9.7 mΩ. Allowing for corrected conduction loss, Fig. 3(a) shows that the standard model (1)-(4) has some inaccuracy in predicting switching loss for this device. Loss measurements, presented in Fig. 3(b), were then taken in 4 parallel-connected IRFP4668 devices in a half-bridge with 3 different values of gate resistance. Again, the standard loss model (1)-(4) does not correctly predict the increase in switching loss with gate resistance.



(a)

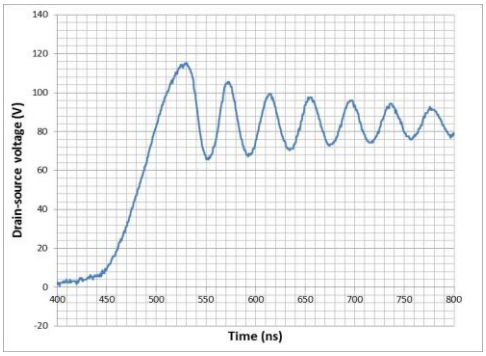


(b)

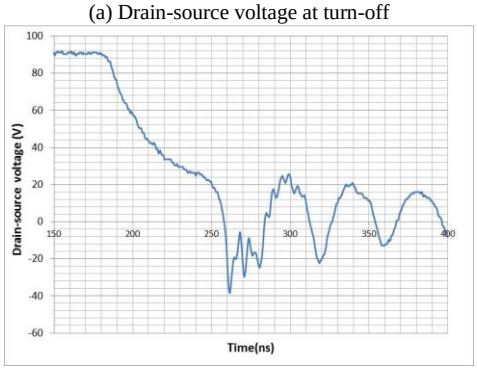
Fig. 3. Measured loss for IRFP4668 devices, compared with equations (1)-(4): (a) Total loss for a single device at 20 kHz compared with the standard Si MOSFET loss model, (b) Total loss at 2 kHz for 4 parallel-connected devices, with varying gate resistance

B. Improved Si MOSFET Switching Loss Model

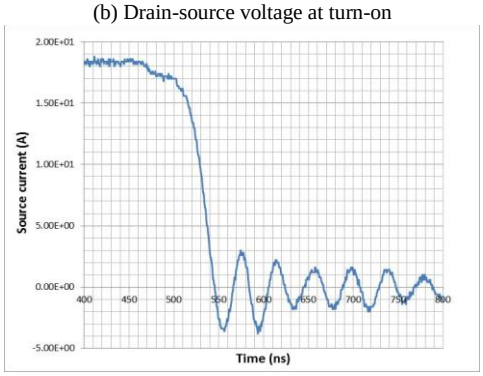
Typical measured switching waveforms are shown in Fig. 4. for Si MOSFET turn-on and turn-off, showing inductance effects caused by rapid switching achieved by these small Si MOSFETs in the TO-247 package. Inductance effects are particularly evident in Fig. 4 (b) where the drain-source voltage transient appears to slow down when it approaches 25 V, whereas in fact this measurement is the voltage across the lead inductance rising as the rate of change of current increases, superimposed on top of the actual device drain-source voltage. It was only possible to attach a Rogowski coil to the source in the PCB layout and hence Fig. 4 presents source current measurements, and therefore includes gate current. In order to improve the accuracy of Si MOSFET switching loss prediction, selected analytical models for SiC MOSFETs [19,20] were examined. These define the switching transitions as a series of stages which are approximated to be linear. This approach was used to develop a similar model for Si MOSFETs. Fig. 5(a) shows the linearized switching transitions for turn-on, and Fig. 5(b) for turn-off. Only the stages in which loss is significant are described in detail.



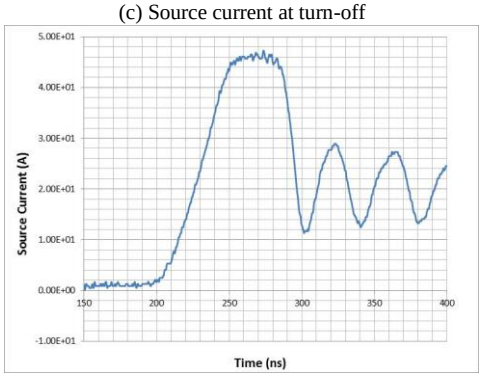
(a) Drain-source voltage at turn-off



(b) Drain-source voltage at turn-on



(c) Source current at turn-off



(d) Source current at turn-on

Fig. 4. Typical measured waveforms for a Si MOSFET

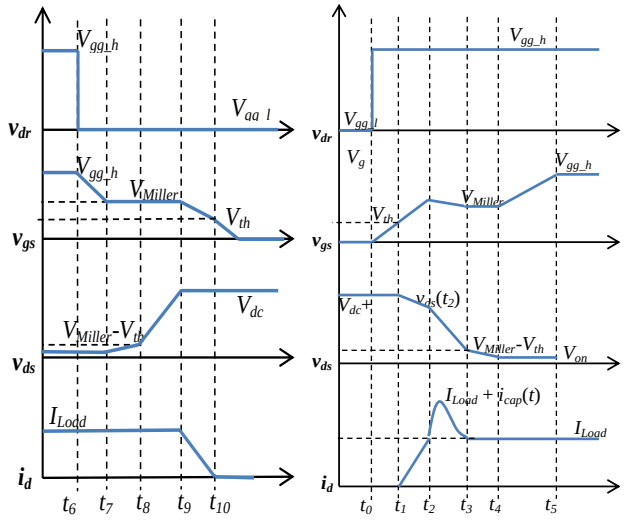
Stage 2: t_1 to t_2: MOSFET channel current rises to reach the value of the load current

In this stage there are no significant changes compared with previous approaches [19], except to allow for parallel connection of k devices. Equivalent gate resistance for each device is given by $R_{eq} = R_{ext} + (R_{gint} + R_{miller})/k$, in which R_{ext} is the output resistance of the gate driver, R_{gint} is the internal gate resistance of a single device, and R_{gp} is the connection resistance of each individual device gate to the gate driver output. The time taken to pass through the transition t_1 to t_2 is given by (5), and the energy lost is given by (6)

$$(t_2 - t_1) = \frac{\left(C_{gs}R_{eq} + g_{fs}\left(\frac{L_s}{k} + L_{ext}\right)\right)}{g_{fs}\left(V_{gg\_h} - 0.5(V_{miller}(k) + V_{th})\right)} I_{load} \quad (5)$$

$$E_{1\_2} = (V_{dc} + V_d)\frac{I_{load}(t_2 - t_1)}{2} - \left(\frac{L_s + L_d}{k} + L_{ext}\right)\frac{{I_{load}}^2}{2} \quad (6)$$

where C_{gs} is gate-source capacitance, L_s is source inductance, and g_{fs} is transconductance, all for a single device. L_{ext} is the inductance of the circuit board track connecting all of the parallel-connected devices, I_{load} is the total load current in all k parallel-connected devices, $V_{miller}(k)$ is the Miller gate voltage necessary for a single device carrying I_{load}/k drain current, V_{gg_h} is the gate drive voltage in the high state, and V_d is the voltage drop across the diode in the opposing device in the half-bridge.



(a) Turn-off (b) Turn-on

Fig. 5. Linearized switching transitions for a Si MOSFET

Stage 3: t_2 to t_3: Output capacitance discharges such that drain-source voltage falls to reach V_{Miller} - V_{th}, (after which point the device will enter the ohmic region)

The first step is to find the drain-source voltage, $v_{ds}(t_2)$, at time t_2, which is given by (7).

$$v_{ds}(t_2) = V_{dc} + V_d - \frac{(L_s + L_d)I_{load}}{k(t_2 - t_1)} - \frac{L_{ext}I_{load}}{(t_2 - t_1)} \quad (7)$$

L_d is the drain inductance of a single device. If, during this phase, gate-source voltage is relatively constant, the following assumptions can be made: gate-drain capacitance, C_{gd}, charging current dominates gate current, and time rate of change of gate-drain voltage, $v_{gd}(t)$, is dominated by changing $v_{ds}(t)$. At the same time, the current in the MOSFET channel is the sum of the load and drain capacitance, C_{oss}, charging currents, $i_{cap}(t)$, allowing gate current to be defined as a function of voltages around the gate-source loop, (8). Here, total gate-drain and drain-source capacitance is the sum of the upper and lower device capacitances, $C_{oss}(V_{dc}\text{-}v_{ds}(t))$ + $C_{oss}(v_{ds}(t))$, and load capacitance, C_L.

$$i_g = \frac{V_{GG} - V_{miller}(k) - \frac{i_{cap}(t)}{g_{fs}}}{R_{eq}} = -C_{gd}\frac{dv_{ds}}{dt} \quad (8)$$

Equation (8) can then be integrated and rearranged to find (t_3 - t_2), which is given by (9).

$$(t_3 - t_2) = \frac{1}{V_{GG} - V_{miller}(k)} \left\{ \begin{array}{c} \frac{2}{g_{fs}} \left[Q_{oss}\left(v_{ds}(t_2)\right) - Q_{oss}\left(V_{miller}(k) - V_{th}\right) \right] \\ + \frac{C_L (V_{dc} - V_{miller}(k) + V_{th})}{g_{fs}} \\ + kR_{eq} \left[Q_{rss}\left(v_{ds}(t_2)\right) - Q_{rss}\left(V_{miller}(k) - V_{th}\right) \right] \end{array} \right\} \quad (9)$$

$Q_{oss}(V)$, $Q_{rss}(V)$ are the total charges in the output and reverse transfer capacitances respectively of a single device at voltage V. Energy lost during this transition is found by integrating the product of current and voltage during this time period. If the voltage across the device which is turning on is plotted as a function of stored charge, Fig 5, then the energy lost as one device is turned off is given by the light grey area, while losses given by the device turning on are given by the dark grey area. The total energy lost is therefore the sum of light and dark grey areas which is equal to the product of the change in total charge stored in the output capacitance of one device and the change in device drain-source voltage.

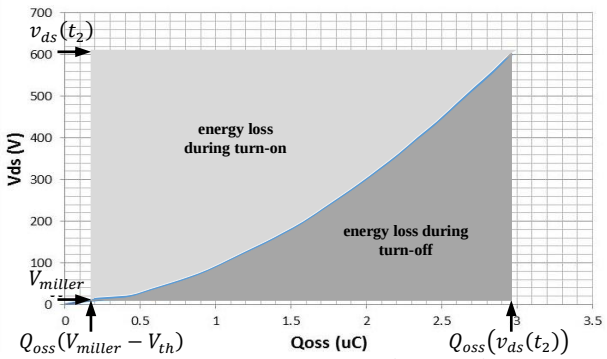


Fig. 6. Integrating drain-source voltage as a function of charge stored in total output capacitance for a half-bridge. The light grey area represents the energy loss associated with increasing charge in the opposing device which is turning off, while the dark grey area represents energy loss associated with removing the charge in the device which is turning on.

Energy removed from the load capacitance, C_L, is calculated using $0.5C_LV^2$ since this is a linear capacitance.

$$E_{2\_3} = I_{load}(t_3 - t_2)\left[\frac{\left(v_{ds}(t_2)\right) + \left(V_{miller}(k) - V_{th}\right)}{2}\right] + k\left(Q_{oss}\left(v_{ds}(t_2)\right) - Q_{oss}\left(V_{miller}(k) - V_{th}\right)\right)\left(v_{ds}(t_2) - \left(V_{miller}(k) - V_{th}\right)\right) + 0.5C_L\left(V_{dc} - V_{miller}(k) + V_{th}\right)^2 \quad (10)$$

Stage 3: Diode reverse recovery loss also takes place during this stage

Diode reverse recovery loss is given by (4) provided that reverse recovery charge can be correctly predicted. Reverse recovery loss measurements were made for the IRFP4668 device over a range of voltages and currents, which demonstrated that Q_{rr} does not vary linearly with voltage and current, see Fig. 7.

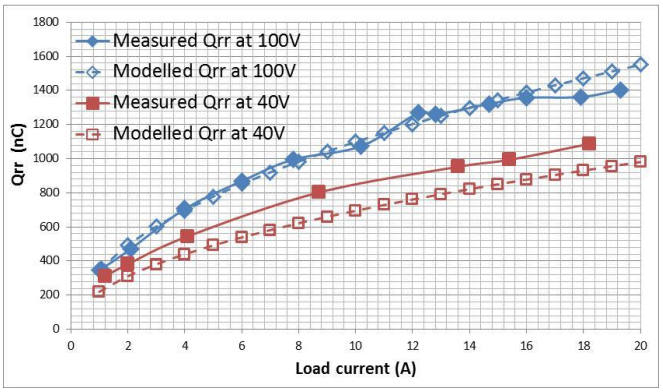


Fig. 7. Measured diode Q_{rr} as a function of current, at 40V and 100V, for the IRFP4668, compared with Q_{rr} predicted using (11)

The first step in improving the prediction of Q_{rr} is to calculate the rate of change of current at MOSFET turn-on using the transition time $(t_2 - t_1)$, so that $di/dt = \frac{I_{load}}{(t_2 - t_1)}$. *di/dt* can then be used to select a more accurate starting value, Q_{rr_nom}, prior to adjusting for load current and DC voltage. The variation with current and voltage was then found approximately over the range of current and voltage of interest using (11). Note that at zero load current reverse recovery charge does not fall to zero due to diode capacitance, and hence (11) is not valid at zero current.

$$Q_{rr} = Q_{rr\_nom}\sqrt{\frac{I_{load}}{kI_{test}}}\sqrt{\frac{V_{dc}}{V_{test}}} \quad (11)$$

I_{test}, V_{test} are the current and voltage at which Q_{rr} is given as a function of *di/dt* in the data sheet.

Stage 4: t_3 to t_4: The device is now in the ohmic region, and drain-source voltage falls to the on-state voltage

Gate voltage is constant during this transition, but now capacitive charging currents are negligible in the MOSFET channel compared with load current so gate current is approximately constant and is given by (12).

$$i_g = \frac{V_{GG} - V_{miller}}{R_{eq}} \quad (12)$$

By setting the integral of gate current equal to the charge removed from this capacitance, the transition time can be found from (13).

$$(t_4 - t_3) \approx \frac{kR_{eq}Q_{rss}(V_{miller} - V_{th})}{V_{GG} - V_{miller}} \quad (13)$$

Loss is then found by integrating the product of voltage and current as for the previous stage, giving (14), assuming that during this stage $V_{on} \approx 0$V.

$$E_{3\_4} = \frac{I_{load}(V_{miller} - V_{th})(t_4 - t_3)}{2} + k(V_{miller} - V_{th})Q_{oss}(V_{miller} - V_{th}) + 0.5C_L\left(V_{miller}(k) - V_{th}\right)^2 \quad (14)$$

Stage 8: t_7 to t_8: The device remains in the ohmic region, and output capacitance charges up to V_{Miller} - V_{th}

Time taken and energy loss can be calculated in much the same way as for Stage 3, giving (15) and (16).

$$(t_8 - t_7) = \frac{R_g Q_{rss}(V_{miller} - V_{th})}{V_{miller} - V_{GG\_L}} \quad (15)$$

$$E_{7\_8} = (t_8 - t_7)I_{load}0.5(V_{on} + V_{miller} - V_{th}) \quad (16)$$

Stage 9: t_8 to t_9: C_{ds} and C_{gd} are charging with C_{gs} constant, while current remains near the full-load value

During this period the gate-source voltage is constant at the Miller voltage. Current at the gate can be equated as (17).

$$C_{gd}\frac{dv_{ds}}{dt} = \frac{V_{gg}-v_{gs}}{kR_{eq}} \quad (17)$$

Integrating both sides of (17) with respect to time, and approximating the rise in drain voltage as V_{dc}, (18) gives the t_8 to t_9 transition time and (19) gives the loss.

$$(t_9 - t_8) = \frac{kR_{eq}Q_{rss}(V_{dc})}{V_{gg}-V_{miller}} \quad (18)$$

$$E_{8\_9} = 0.5(t_9 - t_8)I_{load}V_{dc} \quad (19)$$

Stage 10: t_9 to t_{10}: Channel current falls to zero

Transition time is found by equating gate current with gate-source capacitive charging current and taking the average gate-source voltage to be $0.5(V_{Miller} + V_{th})$, and rearranging to find (20).

$$(t_{10} - t_9) = \frac{kR_{eq}C_{gs}(V_{miller}-V_{th})+L_s\frac{I_{load}}{k}+L_{ext}I_{load}}{V_{gg}-0.5(V_{miller}+V_{th})} \quad (20)$$

Loss is then readily found since the voltage across the device is equal to the DC supply voltage, (21).

$$E_{9\_10} = 0.5(t_{10} - t_9)I_{load}V_{dc} \quad (21)$$

Fig. 8 compares the analytical loss calculated using (5)-(21) with experimental loss data.

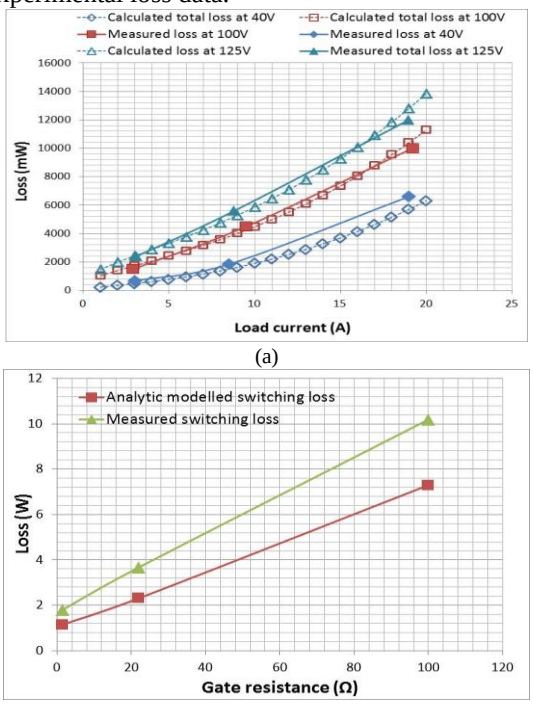


Fig. 8. Measured loss for IRFP4668 devices, compared with equations (5)-(21): (a) Total loss at 20kHz compared with the analytical Si MOSFET loss model (5)-(21), for a single device, (b) Total loss at 2kHz for 4 parallel-connected devices, with varying gate resistance

Agreement in Fig. 8(a) is very good. However, whilst agreement in Fig. 8(b) is a considerable improvement compared with Fig. 3(b), it is clear that the model still significantly underestimates switching loss once the IRFP4668 devices are connected in parallel. This results from different turn-on rates for the different MOSFETs due to different threshold voltages. Once one MOSFET reaches its threshold voltage it quickly starts to conduct the full-load current. At this point it enters the Miller region and the gate-drain capacitance starts to discharge. However, although the other MOSFETs are still in the off-state at this point, the device which switches on first must discharge all of the other gate-drain capacitances as well as its own, which happens at a rate which is slower by an amount equal to the number of devices in parallel. In addition, the discharging current in the gate-drain capacitances of the off-state MOSFETs starves their gate-source capacitances of charging current, increasing their turn-on time still further. This has the effect of slowing the turn-on rate considerably more than predicted by the model, which assumes that all devices connected in parallel are identical.

IV. Si MOSFET Modular Multilevel Converter Losses under Slowed Switching

The model presented in (5)-(21) was used to predict losses for 5-, 7- and 9-level MMC converters, shown in Fig. 9, which are also compared with loss predictions for the optimized SiC 2-level converter. All losses include inductance and capacitance loss, assuming the use of ferrite cored inductors and electrolytic capacitors. While film capacitors would reduce MMC losses by around 15 %, the increase in cost and volume is not acceptable for a low voltage application. The MMC overall switching frequency is taken to be 10 kHz, giving cell switching frequency of 10 kHz / (n+1), where n+1 is the number of levels.

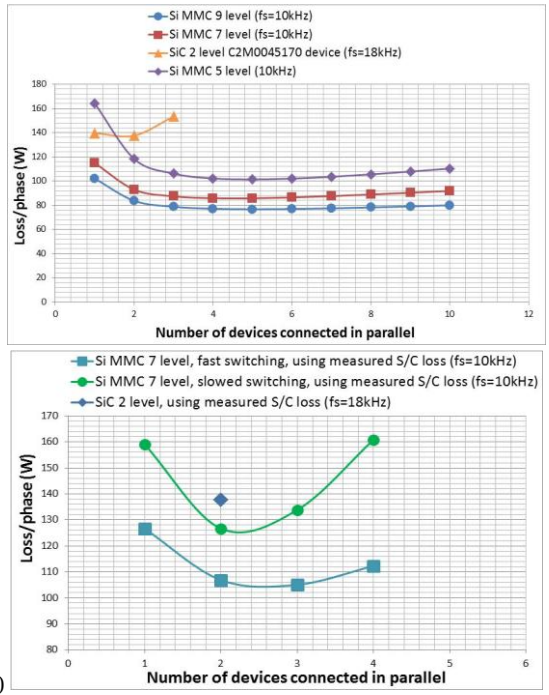


Fig. 9 Calculating converter loss using calculated (a) and measured (b) semiconductor losses: (a) Calculated converter loss for Si MOSFET MMC and SiC 2-level converters. Inductor, capacitor, and semiconductor conduction and switching losses are all included, (b) Using measured semiconductor losses to calculate converter loss.

From Fig. 9(a) it is clear that increasing the number of MMC levels from five to seven gives some improvement in

efficiency, and that further increasing the number of levels results in negligible improvement. Hence 7 has been chosen as the optimal number of levels for the 750 V_{dc} bus, although 5-levels still result in a considerably more efficient converter when compared to an SiC 2-level topology. It is also clear that parallel-connection of more than 4 devices actually deteriorates efficiency, and in fact it is arguable that 2-3 devices in parallel might well be sufficient. However, for the purposes of investigating the effect of parallel-connection on loss and EMI, it is of interest to carry out a practical study into the EMI generated by up to 4 parallel-connected devices as the maximum number of devices that it would be reasonable to connect in parallel.

Semiconductor losses were measured for the SiC half bridge at 600 V, 3.3 kW. The Si MOSFET MMC single cell was measured at 125 V with load current equivalent to that in a full MMC delivering 3.3 kW. Fig. 9(b) shows losses, found using calculated passive losses added to the measured semiconductor losses. For the Si MOSFET MMC, single cell losses are multiplied by the total number of cells to find total MMC converter loss. From Fig. 9(b) it is clear that the spreading of switching times caused by parallel connection means that two, rather than four, parallel-connected MOSFETs are optimum.

V. EMI

Radiated emissions were measured using Tekbox near-field probes with 40-dB wideband amplification, see Fig. 10. Both magnetic fields (*H*-fields) and electric fields (*E*-fields) were measured, with the probe positioned at the same distance from the center of each switching circuit to enable fair comparison of emissions from Si and SiC device based circuits. This method is unsuitable for measuring absolute emissions, and can only be used to indicate comparative emissions from different circuits. Measurements were not unduly sensitive to small lateral movements of the probe, hence the results are likely to give a reasonably realistic indication of relative EMI in SiC and Si MMC converters. DC-100 MHz presents the most critical section of the frequency range [23], however, for clock frequencies below 1.705 MHz the upper frequency of measurement is given in the FCC Part 15.33 as 30 MHz for radiated emissions. Therefore, with switching frequencies of 10 kHz and below radiated emissions have been measured up to 50 MHz in this work, with some plots to 100MHz for illustrative purposes. Conducted emissions were measured over the DC-30 MHz range as required by the FCC (note that the FCC and CISPR measurement frequency ranges are very similar, although there is some difference in the maximum emission threshold at any given frequency).

Near-field measurements would be meaningless in a full MMC converter, since the near field probe can only be near one MMC cell at a time. Hence a single MMC cell was measured for the Si MMC. Assuming that the switching transition primarily contains a fundamental frequency of f_T, then harmonics are generated at ($\pm mf_T \pm nf_{sw}$), where m and n are whole numbers (including 0), and f_{sw} is switching frequency. Hence, as f_{sw} increases, so do the frequencies of many of the harmonics. *E*-fields are generated through both differential and common-mode currents, with common-mode currents tending to dominate EMI radiation [24]. *E*-fields from common-mode currents are proportional to both frequency and current magnitude, while *E*-fields from differential-mode currents are proportional to the square of frequency [25]. Consequently, increasing switching frequency increases EMI amplitude. The EMI spectrum is the result of harmonic mixing which can only take place inside a nonlinear component such as a MOSFET or a diode. The frequencies present in these components therefore generate the EMI spectrum and dominate its amplitude. Each rapid switching transition generates a harmonic spectrum which is independent of the switching frequency, and in which the frequency is dictated by rate of change of voltage and current. These transition related harmonics then mix with the switching frequency in the nonlinear switch. Each switching device in the MMC sees only the cell switching frequency, and hence spectral content is constructed from the transition generated spectrum combined with the cell switching frequency. Each MMC cell produces approximately equal harmonic content, but phase shifted since the cells switch at different instants in time. At any instant in time therefore, emissions are generated from a single MMC cell only, and hence it is not expected that the EMI level should increase in proportion to the number of cells. The effect of accumulating numbers of MMC cells is quantified as well as is practically possible in this paper by comparing EMI from a single cell, with and without the presence of a second cell.

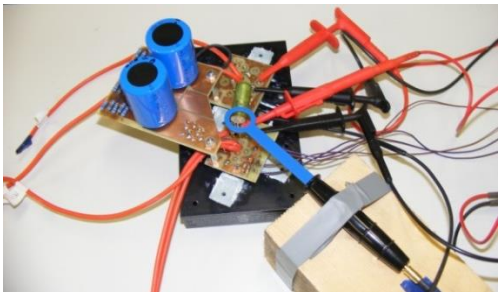


Fig. 10. Measuring EMI from the SiC 2-level converter using Tekbox near-field probes (*H*-field probe pictured).

The switching frequency for EMI measurements on the Si MMC single cell has been taken to be $f_{sw} / (n+1) = 1.43$ kHz since f_s=10 kHz and with 7 MMC levels n=6. However, adjustment must be made to account for the fact that with the SiC converter the EMI emitted by a complete phase is under measurement, whereas the single MMC cell indicates EMI for only one arm of a phase. Adjustment can be made by assuming that the EMI from both arms will sum perfectly in phase, so that the EMI from the complete phase will be 6 dB greater than that for a single arm. This is the worst case, but it will be seen that even with this pessimistic assumption, Si MMC EMI is lower than that for the SiC 2-level converter.

Conducted emissions were compared by applying a Fast Fourier Transform (FFT) to both drain-source voltage and source current waveforms. While the DC voltage is ideally 750 V, as chosen in Section I, power supply availability meant

that the SiC 2-level converter was measured operating from 600 V_{dc} instead. This slightly reduces the EMI from the SiC circuit, but since the Si MMC will be seen to produce lower EMI even when the SiC converter operates from 600 V, this restriction is not considered to influence the outcome of the research.

A. Comparison of EMI Measurements

1) Initial comparison of EMI for Si and SiC devices under equivalent operating conditions

Gate resistance definitions are shown for the parallel-connected Si MOSFETs in Fig. 11, and the value of the external shared gate resistor, R_g, is used to adjust switching speed. Si MOSFET and SiC half-bridge switching was therefore compared with 125 V_{dc}, 19 A load current, switching at 2 kHz, and the results can be seen in Fig. 12.

Conducted emissions and radiated *E*-field from the SiC converter are uniformly significantly higher than the Si MMC cell across the band, however, radiated *H*-field is slightly higher from the Si MMC than the SiC converter when external gate resistance is set to 1.5 Ω. The reduction in emissions brought about by increasing the gate resistance from 1.5 Ω to 22 Ω is clear from all plots, although there is some slight increase in low frequency *H*-field. However, although the operating conditions for the two circuits are similar, the SiC gate driver switches faster than the Si gate driver which seems likely to explain much of the increased emissions from the SiC. However, this fast gate drive is necessary to achieve acceptable switching losses in the SiC converter.

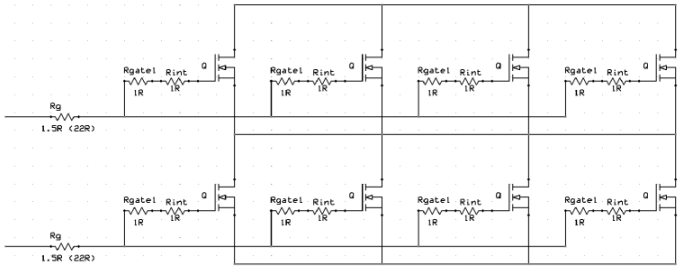


Fig. 11. Parallel connection of 4 MOSFETs showing all gate resistances

2) Impact of switching frequency choice on EMI levels

Whilst changing the switching frequency does not affect the frequency content contained within the spectrum generated by an individual switching transient, the switching harmonics mix with the fundamental switching frequency to generate intermodulation products across the EMI band. With a higher switching frequency the frequencies of the intermodulation products increase in proportion. The Si MMC operates with an effective switching frequency equal to the main switching frequency divided by the number of levels. The stepped output waveform means that the main switching frequency can be low when compared with a 2-level converter, resulting in EMI harmonics occurring at lower frequencies, and consequently having smaller amplitude. The resulting increase in EMI between the Si MOSFET MMC and the SiC converter is therefore expected to be of the order of 20log(18/1.43) = 22 dB assuming that all EMI is dominated by common-mode currents.

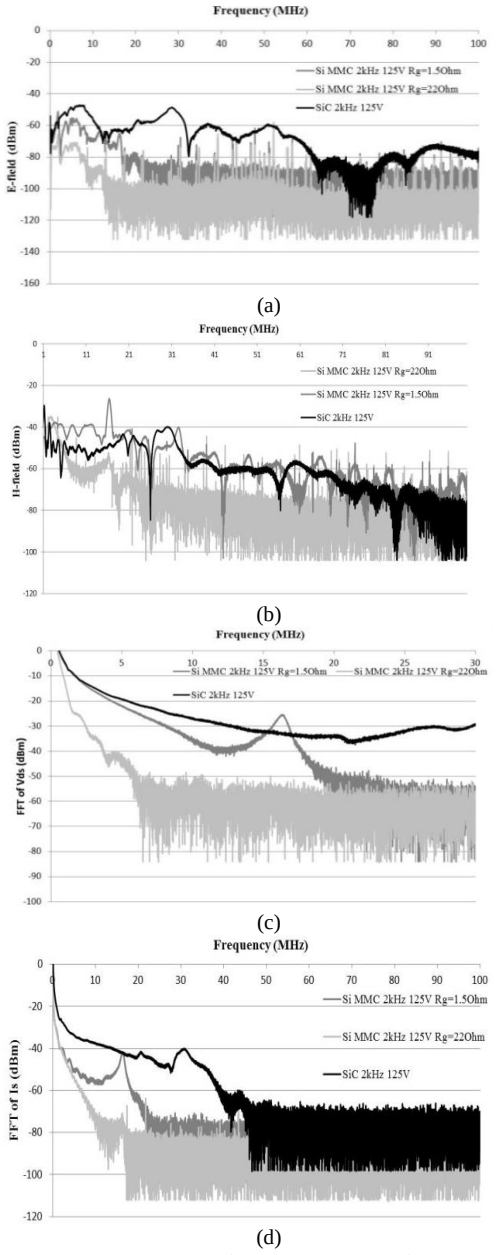


Fig. 12. Comparing (a) radiated *E*-field, (b) radiated *H*-field, (c) voltage noise and (d) current noise from SiC (black) and Si (light grey: slowed switching, dark grey: fast switching) half-bridge cells, all at 125V, 19A, 2kHz. No parallel connection for SiC devices, 4 devices in parallel for Si MOSFET.

The effect of changing switching frequency on radiated EMI from the SiC half-bridge can be seen in Fig. 13 where switching frequencies of 10 kHz, 20 kHz and 36 kHz are compared. Expected increase in EMI from 10 kHz to 20 kHz would be 20log(2) = 6 dB for common-mode generated harmonics, and $20\log(2)^2$ = 12 dB for differential-mode harmonics. Since the difference appears to be mainly 6 dB it would appear that common-mode generated harmonics dominate the radiated spectrum. It should be noted that the general envelope of the spectrum is not affected by switching frequency, although in practice individual harmonics have moved by the expected frequency shift. This is explained by the fact that the spectrum consists of harmonics which are independent of switching frequency, being determined by

MOSFET switching speed, and which are then modulated by the switching frequency. The shape of the envelope is therefore determined by the frequency content within the switching transient, and the amplitude of the spectrum is determined by the switching frequency (for a given semiconductor technology, PCB layout, and gate driver circuit).

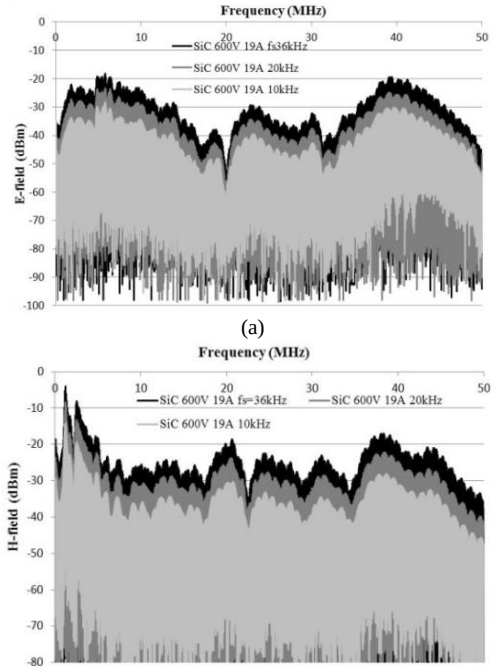


Fig. 13. Examining the effect of switching frequency on (a) *E*-field and (b) *H*-field, for SiC half bridge, f_s=38 kHz (black), f_s=20 kHz (dark grey), f_s=10 kHz (light grey)

3) Effect of slowed switching in Si MMC cell.

The theoretical effect of slowed switching can be estimated by considering that the relationship between the rate of change of current and the frequency content of the EMI spectrum is approximately linear. Hence, when external gate resistance R_g is varied from 22 Ω to 1.5 Ω, with internal resistances accounted for, EMI is expected to increase by approximately 20log(22/3.5) = 16 dB, see Fig. 14. The predicted EMI reduction is seen generally across the frequency band in *E*-field and conducted voltage measurements. It should be noted how slowed switching has less impact than expected on both radiated *H*-field and the current waveform. This is because gate loop inductance has a dominating effect on gate-source impedance during the period where channel current is falling (Stage 10 switching as described in Section III.B), which can be seen in (19) where the $kR_{eq}C_{gs}(V_{miller}-V_{th})$ term is much smaller than the $(L_{ext} + L_s/k)I_{load}$ term until such time as the external gate resistance is excessively large. Increasing gate resistance does slow down turn-on current rise however (the $R_{eq}C_{gs}$ term dominates the numerator of (5)), and so there is still some reduction in *H*-field and conducted current harmonics as gate resistance is increased. Current waveforms at turn-on and turn-off are shown in Fig. 15 for fast and slow switching. Current related EMI is further complicated by the fact that ringing is reduced with slowed switching (see Fig. 15), leading to a reduction in the density of the EMI response, particularly visible in the radiated *H*-field, but less so in the FFT of I_s because the harmonics are partly obscured by the noise floor: note that, as a result of large fundamental current amplitude, it was not possible to lower the noise floor with the test set-up used to carry out this initial relative assessment of EMI.

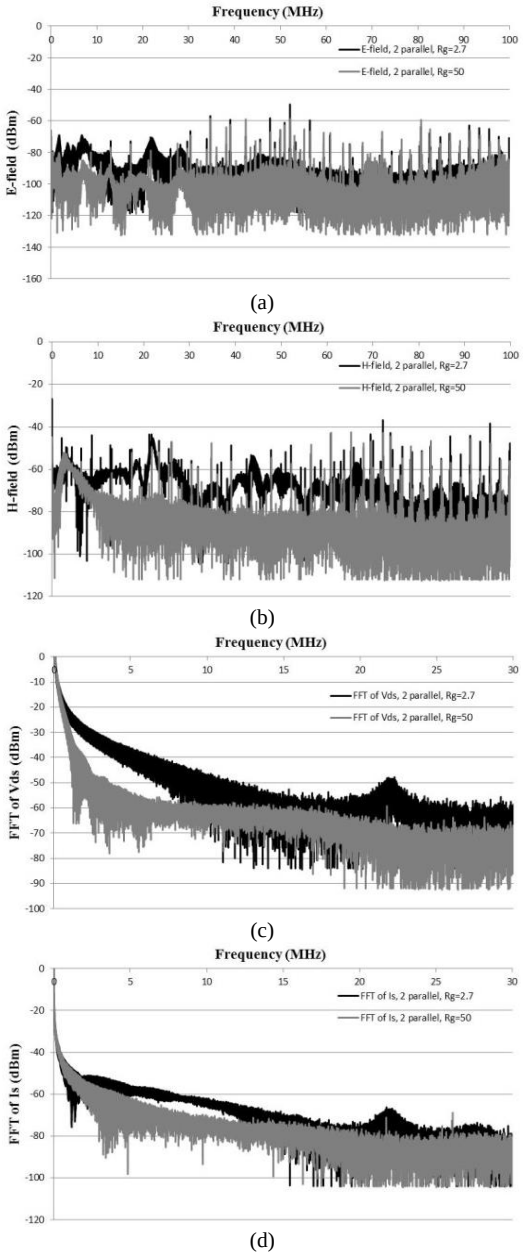
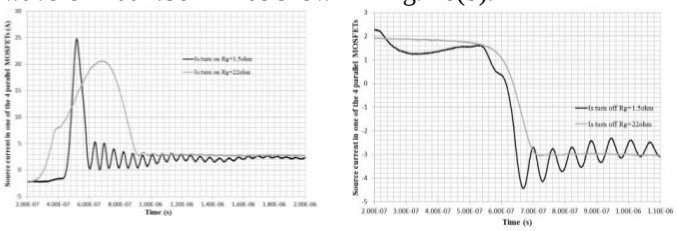


Fig. 14. Comparing (a) radiated *E*-field, (b) radiated H-field, (c) voltage noise and (d) current noise from Si MMC, with 2 parallel-connected devices, at 1.43 kHz with fast switching (black) and slowed switching (grey), at 125 V, 11.4 A.

4) Measuring the effect of a second cell on EMI

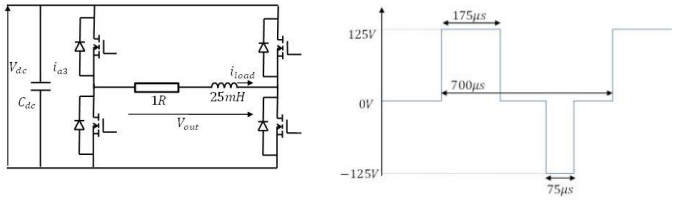
In the MMC, multiple cells are connected in series (see Fig. 8) through which the same load current flows. As discussed in Section V.A, the mechanism for generating EMI at the overall switching frequency is limited in the MMC, although it is possible that some small increase in EMI might be observed as more cells are added.

In order to assess this effect, two MMC cells constructed from IRFP4668 Si MOSFETs, using two parallel-connected devices for each switch, were connected together via a load in an H-bridge arrangement, see Fig. 16(a). They were then switched with interleaved pulse waveforms at 1.43 kHz, in such a manner that the load was subjected to a stepped waveform at 2.86 kHz as shown in Fig. 16(b).



(a) (b)

Fig. 15. Effect of 1.5-Ω gate resistance (black) and 22-Ω gate resistance (grey), on rate of change of Si MOSFET source current, measured using a Rogoswki coil (DC offset has not been adjusted) at (a) Turn on, and (b) Turn off



(a) (b)

Fig. 16. (a) Two MMC cells sharing a common load, and (b) Voltage waveform across the load

This asymmetric waveform, together with the load dimensioning, ensured that the load current was 11.4 A, which is equal to the rms load current in one phase of the 10-kW MMC AC/DC converter delivering 750 V_{dc} from 240 V_{rms} input. EMI from one of the cells operating alone at 125 V / 11.4 A was measured. EMI measurements were then repeated for both cells switching together. The near-field probe retained the same position throughout, and oscilloscope and FFT settings were identical during both sets of measurements. The results are presented in Fig. 17 which shows the measured *E*- and *H*-field, and FFTs of V_{ds} and I_s for one of the switches.

Only the *E*-field spectrum shows a slight rise as a result of the presence of the second cell, where an increase in the region of 6-10 dB is apparent at some frequencies: particularly in the 5-20 MHz and the 30-50 MHz frequency bands. It should also be noted that there is a decrease of 10 dB in the region of 20 MHz. In the current spectrum, the peak at 20 MHz appears to have split into two peaks at 15 MHz and 22 MHz, although the amplitude has not changed significantly.

These results appear to confirm the theory that EMI from multiple MMC cells does not replicate EMI which would be expected from operation at the overall switching frequency. The benefits of the cells running at $f_{sw}/(n+1)$ appear in an EMI spectrum which barely changes as a second cell is added to the first. The slight changes (*E*-field amplitude increase at some frequencies, and decrease at others) is attributed to the *E*-field generated by the load at overall switching frequency, and perhaps also some noise from the second cell appearing in the measured cell, but at much lower magnitude than the cell switching frequency.

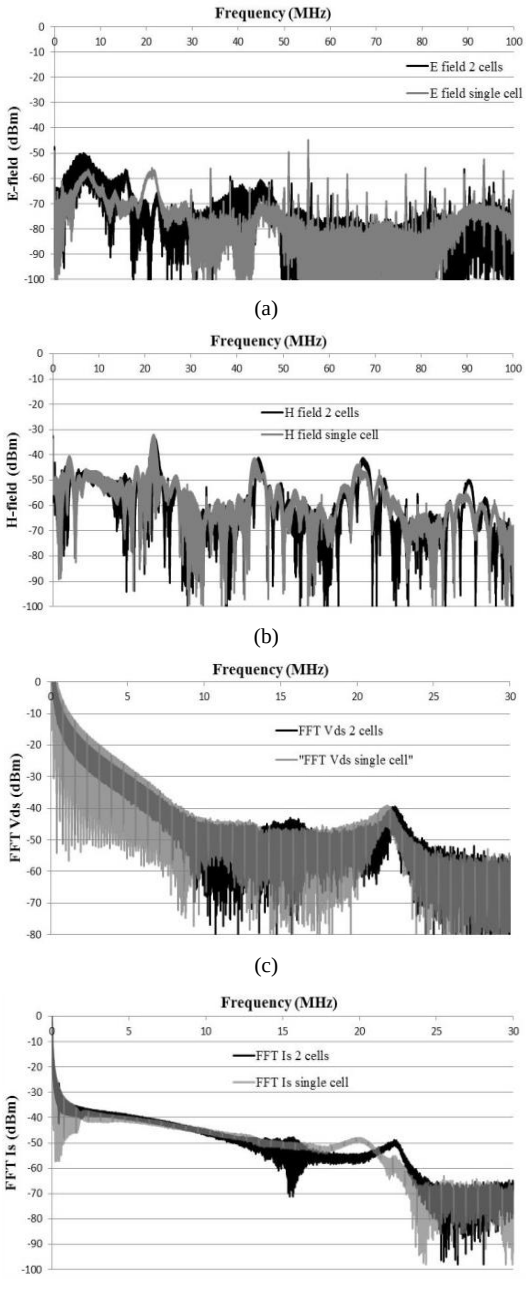


Fig. 17. Comparing (a) radiated *E*-field, (b) radiated *H*-field, (c) voltage noise and (d) current noise from an Si MMC, with two parallel-connected devices, at 1.43 kHz, 125 V and 11.4 A. Comparison is between a single cell (black) and two cells switching a shared load (grey)

5) Comparisons between Si and SiC EMI

Fig. 18 compares measured EMI for the Si MMC, increased by 6dB to account for the second phase arm, with EMI from the SiC 2-level converter. The MMC cell was measured at 125 V, corresponding to a 7-level MMC operating at 750 V_{dc}, and the SiC converter was measured at 600 V_{dc} (due to the power supply restrictions mentioned in Section V.A). Both were measured switching at 50 % duty cycle and both converters were compared at a current equivalent to the

average current delivered by one phase of a 3-phase 10 kW converter.

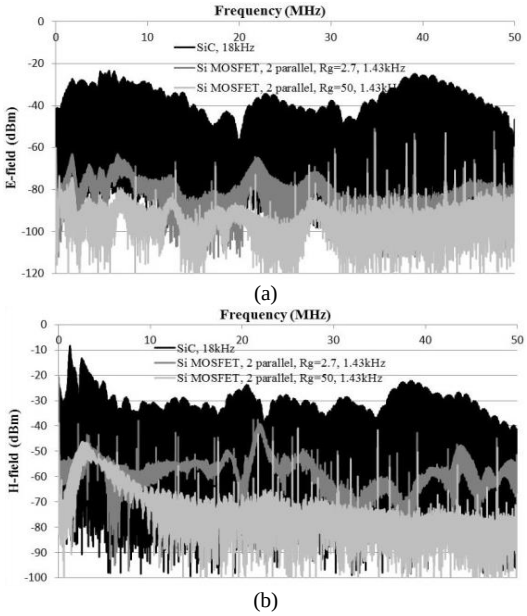


Fig. 18. Comparing (a) radiated *E*-field, (b) radiated *H*-field for an SiC 2-level converter and an Si MOSFET 7-level MMC. SiC 2-level converter: 600 V_{dc}, 10/3 kW, f_{sw}=18 kHz. Si MMC: 125 V/cell, 10/3 kW equivalent, f_{cell}=1.43 kHz (f_{sw}=10 kHz equivalent). Si MMC measurements based on a single cell at the correct voltage for the 7-level converter, and adjusted to allow for a second arm switching simultaneously

Ignoring the effect of slowed switching to begin with, the lower *E*-field in the Si MMC when compared with the SiC 2-level converter can be attributed to two factors. The first is reduced effective switching frequency which leads to a reduction in EMI of 20log(38/1.43) = 28.5 dB, and the second is the reduced amplitude of switching transitions leading to a further EMI reduction of 20log(600/125) = 13.6 dB. Total expected reduction in *E*-field and harmonic content on drain-source voltage between the Si MMC and the SiC 2-level converter is 42 dB, less 6 dB to account for the second MMC arm, leading to a difference of approximately 36 dB. Measured reduction in *E*-field and harmonic content in V_{ds} ranges from approximately 25 dB to 50 dB, with the exception of some harmonics which are at least 10 dB lower. However, it must be noted that this simplified prediction of EMI reduction ignores the different ringing responses. The most significant ringing in both converter designs takes place on the drain-source voltage from which, in particular, the rapid rate of change of voltage contained within the ringing translates directly into the *E*-field spectrum. Hence any differences in switching response caused by variations in both device and PCB parasitic parameters can have a noticeable impact on EMI. However, Fig. 18 shows that slower switching in the Si MMC, together with its lower effective switching frequency and smaller switching transient amplitude, all combine to result in *E*-field levels which are significantly lower than those from a SiC 2-level converter. Incorporating slowed switching to the Si MMC then offers a further *E*-field reduction to better than 50 dB with the exception of a few harmonics which are still approximately 10 dB lower than the SiC *E*-field response.

Examining the *H*-field comparisons, it can be noted that current in a single Si MMC cell is lower than that in the SiC 2-level converter, but once the second phase arm is considered then current switching is effectively higher in the Si MMC than in the SiC converter. SiC current is 13.9 A while for a single Si MMC arm it is 11.4 A (combining DC and AC contributions), to deliver 10/3 kW from a single phase. The combination of reduced switching frequency and slightly reduced current for a single arm gives 30 dB attenuation, which is reduced to 24 dB once a second arm is added. Measured *H*-field reduction varies from approximately 10 dB to 40 dB, including all of the isolated harmonics. Some of the increased EMI reduction of 50 dB compared with the prediction of 24 dB arises from the very high current gate drive on the SiC converter which leads to very rapid current transitions. This high current gate drive is critical to achieving the efficiency measured for this SiC converter, and cannot be compromised without unacceptable loss increase. Slowed switching then provides useful further *H*-field reduction of up to 30 dB.

VI. Volume and Cost Considerations

Volume and cost for the 7-level Si MMC and 2-level SiC converters are compared in Tables I and II respectively.

Total semiconductor losses in a single phase of the 7-level MMC converter amount to 22 W, using two parallel connected devices for each switch, which equates to 48 MOSFETs per phase. For the IRFP4668, junction to ambient thermal resistance, $R_{\vartheta ja}$ = 40 °C/W [22], and assuming a worst case ambient temperature of 40 °C, and remaining below a junction temperature of 125 °C, no heatsink is required for the 7-level MMC converter. The total PCB volume for the 144 MOSFETs included in the 3-phase converter is around 342 cm^3. It can be seen in Table I that the impact of parallel-connecting two devices to reduce losses on converter volume is relatively low since inductor and capacitance volume dominates. The converter cost with two parallel-connected devices is around 13% greater than with single devices.

For the C2M0045170D SiC MOSFET [26] in a 2-level converter with two parallel-connected devices, or 4 devices per phase, total semiconductor losses are 26 W. Assuming the use of Sil-Pad K-6 insulating pad cut for the TO-3P package (which is compatible with the TO247 package) [27], case to heatsink thermal resistance, $R_{\vartheta cs}$ = 0.82 °C/W, and junction to case thermal resistance, $R_{\vartheta jc}$ = 0.24 °C/W [26], then (22) can be used to calculate the required heatsink thermal resistance.

$$R_{\theta sa} = \frac{1}{4}\left[\frac{T_j - T_a}{P_{device}} - R_{\theta jc} - R_{\theta cs}\right] = 3\ °C/W \qquad (22)$$

Using the FISCHER ELEKTRONIK SK 81/ 75 SA heatsink [28] this requires a heatsink volume of 75 cm^3. The additional volume required for the PCB with the SiC MOSFETs would be around 36 cm^3.

The 7-level Si MMC cell capacitance for a 3-phase converter can be calculated using (23) [29], in which $|S|$ is apparent power (VA), V_{DC} is dc voltage (V), V_{cell} is cell voltage (V) and ΔV is the maximum tolerable voltage ripple (V).

$$C_{cell} \geq \frac{1.22|S|}{3\omega V_{DC} V_{cell} \Delta V} \qquad (23)$$

With 10 kVA apparent power, 750 Vdc and ripple limit of 0.1, cell capacitance must be at least 1.4mF, and each phase requires 12 of these capacitors. Using two parallel EPCOS B43630B2687M0 (giving optimum volume to ESR ratio) this leads to a capacitance volume of 1080 cm^3. For the SiC 2-level converter, the dc-link capacitance should be sized at around 160 µF [31], using two series connected electrolytic capacitors such as the Vishay MAL215919331E to achieve over 750Vdc rated voltage this leads to a capacitor volume of around 28 cm^3.

Arm inductance for the MMC can be calculated by adapting the approach outlined in [25] for a 3-phase converter, giving arm inductance of 700 µH to limit 2nd harmonic circulating current to less than 5 % of dc-side current. Using the core design in [21] this requires a total of six E110/56/36 cores for the 3-phase converter, which is a volume of 1890 cm^3. In [21] the ac-side inductance requirement for the SiC 2-level converter is found to be 2 mH for a switching frequency of 18 kHz, and using the same inductor design approach this leads to the same inductance volume of 1890 cm^3.

Using similar costs to those outlined in [32], the total costs for the 7-level Si MMC and 2-level SiC converters are approximated in Table II.

TABLE I
COMPARING VOLUME

	Volume (cm^3)				
	inductors	capacitance	heatsink	switches	**Total**
7-level/ Si MMC	2640	1080	0	342	**4062**
2-level SiC	2640	28	225	36	**2929**

This cost and volume analysis does not include the extra EMI filtering and shielding that would be required for the SiC converter. EMI filtering and shielding volume and cost are challenging to predict without subjecting the design to full EMC qualification, and hence this element has been neglected in this comparison. The impact of EMI qualification on the cost of the SiC 2-level converter seems likely to be significant [33], and may well lead to an increased cost in the SiC converter compared with the Si MMC converter. However, even with EMC qualification the SiC 2-level converter may remain physically smaller than the 7-level Si MMC converter, although the difference will become less significant, however this disadvantage must be weighed against the higher efficiency offered by the 7-level Si MMC converter.

TABLE II
COMPARING COST

	Cost (£)			
	inductors	capacitance	MOSFETs	**Total**
7-level/ Si MMC	380	1043	439	**1862**
2-level SiC	380	48	854	**1282**

Although the MMC converter is a complex circuit structure, it is formed by repetition of standardized simple MOSFET bridges using well established technology. The complexity is largely in control which can be implemented on standard controllers. Additional voltage measurements are required for capacitor balancing but these may be relatively cheap, low bandwidth devices. The complexity of the MMC topology nevertheless has a potential impact on reliability. However, this must be weighed against the potential reliability improvements brought by reduced component stress resulting from slowed switching transients, reduced overshoot, and low operating temperature. An initial reliability comparison between Si MMC and SiC 2-level converters is presented in [11], which expands on the comments made on the subject of SiC reliability in Section I of this paper. With modern PCB processes, the increased quantity of gate-drive requirements are economically and reliably addressed since the drive requirements of slow-switched Si MOSFET are simple when compared with the dual polarity, very rapid switching, high output current gate-drive requirements of SiC.

VII. CONCLUSION

Si MOSFETs are inherently suitable for parallel connection, and with the dominance of conduction losses in MMC, parallel connection is attractive. However, there is a lack of published data on the effect on Si MOSFET switching losses as parallel connection is increased. Switching losses in Si MOSFETs are presented here for up to 4 devices connected in parallel, and correlation with switching loss models is examined. A superior Si MOSFET switching loss model is presented, and the ability of this more accurate model to track parallel connection is examined. While this new model tracks parallel connection much better it is found that the effect of variable gate threshold voltage still leads to some errors in the effect of gate resistance on switching loss with 4 parallel-connected devices.

Low voltage Si MOSFET based MMC offer an efficient alternative to the SiC 2-level converter. EMI from SiC converters is a potential concern due to the fact that low switching losses are achieved through very rapid switching transitions. At the same time, ‘snappy’ diode reverse recovery in Si MOSFETs causes concern for EMI from LV Si MMC. Relative EMI and efficiency measurements on equivalent partial converters have been presented here showing that an Si MMC offers slightly superior efficiency even with slowed switching transitions compared with an SiC 2-level converter, resulting in significantly lower EMI. It is emphasized that these EMI measurements are relative and cannot be used to predict EMI compliance, rather these EMI results provide an indicative comparison between SiC MOSFET and Si MOSFET based low voltage converters.

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